DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	[illegible]	APPD
1	—	10-2-74	LRE IRE	RWF MTS RFG
2B1	—	12-31-75	APPL LRE	CE LEG RFG

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SYMBOL MANUFACTURING REFERENCES NOTES USED-ON TABLE CURRENT DRAIN RECORD OF CHANGES	1	2
CIRCUIT SCHEMATIC	2	2
	3	2
COMPONENT LIST CIRCUIT DESCRIPTION	4	2

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE
				/

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR −(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

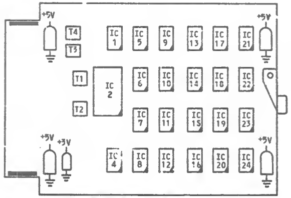
IC CODE	BAT. TERM.	GRD TERM.
41BP	16	8
41CF	16	7,8
175H	1,32	16,17
KS-21688 L1	14	7
KS-21688 L3	14	7
KS-21688 L4	14	7
KS-21688 L5	14	7
KS-21688 L6	14	7
KS-21687 L1	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	006,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

6. INTEGRATED CIRCUIT AND TRANSFORMER LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

CURRENT DRAIN: 600mA

SYMBOL

SERIAL PERIPHERAL INTERFACE B
ELEMENT IDENT
A

TERM. MOD	FUNCT	TERM.	LOC
101ST0	I	309	2A7
INF000	I	215	2A7
INF010	I	314	2A7
INF020	I	211	2A6
INF030	I	310	2A6
INF040	I	116	2A5
INF050	I	214	2A5
INF060	I	205	2A4
INF070	I	304	2A4
INF080	I	301	2A4
INF090	I	003	2A3
INF100	I	010	2A2
INF110	I	109	2A2
INF120	I	207	2A2
INF130	I	307	2A1
INF140	I	312	2A1
INF150	I	212	2A0
INFPH0	I	203	2A0
INFPL0	I	206	2A3
MYRAN	I	311	3A0
MYRAP	I	213	3A0
MYRBN	I	208	3A1
MYRBP	I	308	3A0
PLIØB0	I	317	2A0
RSET01	I	006	3A3
STRTR1	I	217	3A7
B000	Ø	113	2G7
B010	Ø	014	2G7
B020	Ø	100	2G6
B030	Ø	117	2G6
B040	Ø	016	2G5
B050	Ø	101	2G5
B060	Ø	001	2G4
B070	Ø	104	2G4
B080	Ø	008	2G3
B090	Ø	313	2G3

TERM. MOD	FUNCT	TERM.	LOC
B100	Ø	114	2G2
B110	Ø	103	2G2
B120	Ø	[illegible]	2G2
B130	Ø	[illegible]	2G1
B140	Ø	018	2G1
B150	Ø	002	2G0
BPH0	Ø	102	2G0
BPL0	Ø	107	2G4
MYSAN	Ø	118	3H0
MYSAP	Ø	218	3H0
MYSBN	Ø	219	3H1
MYSBP	Ø	318	3H1
RSNP0A	Ø	105	2G6
SCB010	Ø	017	2G7
SCB020	Ø	115	2G7
SPE1	Ø	315	3H7
STØP80	Ø	005	2G8
3VI	Ø	201	309
+5	P	000,119	3H5
GRD	G	200,319	3H7

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	CPS-JK6
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE).	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE
2B1

1N9B

JK6 CIRCUIT PACK

SERIAL PERIPHERAL INTERFACE B
CIRCUIT

②

AT&TCO
STANDARD

CPS-JK6
4 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

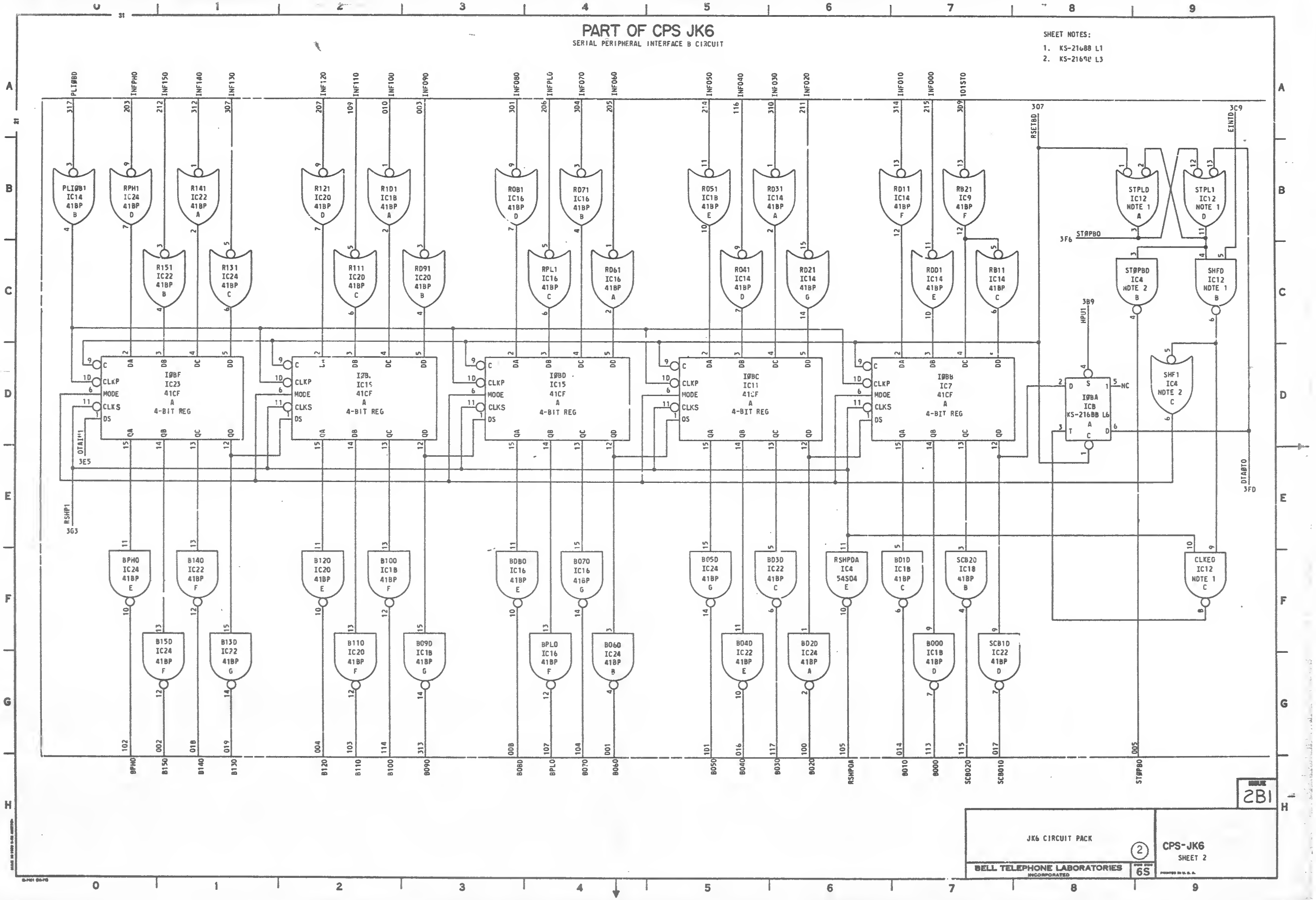
6S

PART OF CPS JK6

SERIAL PERIPHERAL INTERFACE B CIRCUIT

SHEET NOTES:

1. KS-21688 L1
2. KS-21690 L3



CPS-JK6

2B1

JK6 CIRCUIT PACK ②

BELL TELEPHONE LABORATORIES
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CPS-JK6
SHEET 2

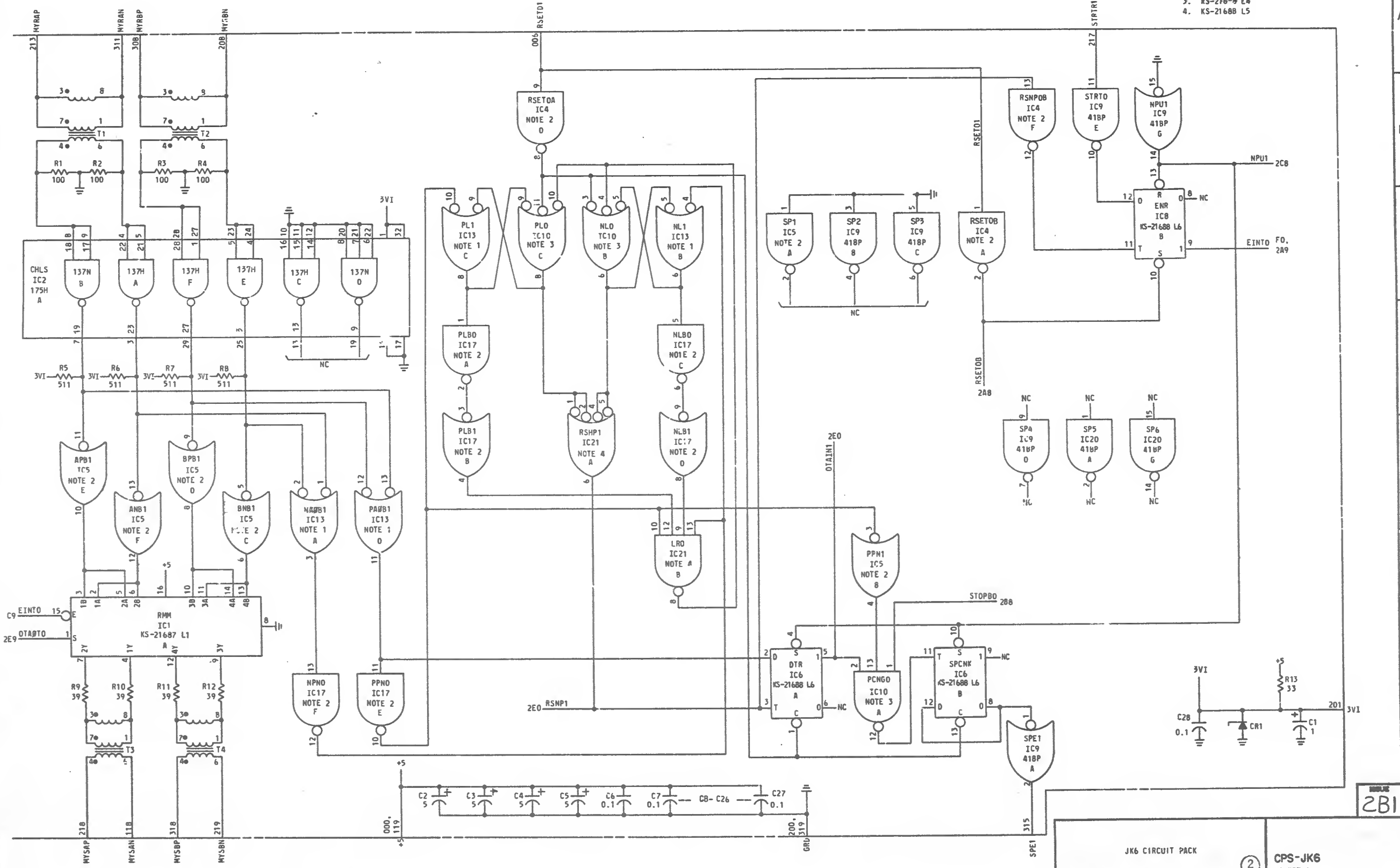
PRINTED IN U.S.A.

PART OF CPS JK6

SERIAL PERIPHERAL INTERFACE B CIRCUIT

SHEET NOTES:

1. KS-21688 L1
2. KS-21688 L3
3. KS-216°9 L4
4. KS-21688 L5



JK6 CIRCUIT PACK

②

BELL TELEPHONE LABORATORIES
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CPS-JK6
SHEET 3

ISSUE 2B1

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PART OF CPS JK6

SERIAL PERIPHERAL INTERFACE B CIRCUIT

COMPONENT LIST

INTEGRATED CIRCUIT

LOC	IC1		IC2		IC4		IC5		IC6		IC7	
CODE	~~54S158~~ KS-21687 L1		175H		~~54S04~~ KS-21688 L3		~~54S04~~ KS-21688 L3		~~54S74~~ KS-21688 L6		41CF	
ELEM IO	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	RMM	3F0	CHLS	3C0	RSETOB	3C7	SP1	3C5	OTR	3G5	IOBB	2D7
B					STOPB0	2C8	PPH1	3F6	SPCHK	3G6		
C					SHF1	2D9	BNB1	3E1				
O					RSETOA	3B3	BPB1	3E1				
E					RSHPOA	2F5	APB1	3E0				
F					RSHPOA	3B7	ANB1	3E0				
C												

LOC	IC8		IC9		IC10		IC11		IC12		IC13	
CODE	~~54S74~~ KS-21688 L6		41BP		~~54S10~~ KS-21688 L4		41CF		~~54S00~~ KS-21688 L1		~~54S00~~ KS-21688 L1	
ELEM IO	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	IOBA	2D8	SPE1	3H7	PCHGO	3C6	IOBC	2D5	STPLO	2B8	NAOB1	3E2
B	ENR	3CB	SP2	3C6	NLO	3C4			SHFO	2C9	NL1	3C4
C			SP3	3C6	PLO	3C3			CLKEO	2F9	PL1	3C3
O			SP4	3E7					STPL1	2B9	PAOB1	3E2
E			STRTO	3B7								
F			RB21	2B7								
C			HPU1	3B8								

LOC	IC14		IC15		IC16		IC17		IC18		IC19	
CODE	41BP		41CF		41BP		~~54S04~~ KS-21688 L3		41BP		41CF	
ELEM IO	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	R031	2B6	IOBD	2D4	R061	2C4	PLBO	3D3	R101	2B2	IOBE	2D2
B	PLIOB0	2B0			R071	2B4	PLBL	3E3	SCB20	2F7		
C	RB11	2C7			RPL1	2C4	NLBO	3D4	B010	2F7		
O	R041	2C5			R081	2B3	NLB1	3E4	B000	2F7		
E	R001	2C7			B080	2F4	PPHO	3G2	R051	2B5		
F	R011	2B7			BPLO	2F4	NPHO	3G2	B100	2F2		
G	R021	2C6			B070	2F4			B090	2F3		

LOC	IC20		IC21		IC22		IC23		IC24	
CODE	41BP		~~54S40~~ KS-21688 L5		41BP		41CF		41BP	
ELEM IO	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	SP5	3E7	RSHP1	3E4	R141	2B1	IOBF	2D1	B020	2F6
B	R091	2C3	LRO	3F4	R151	2C1			B060	2F4
C	R111	2C2			B030	2F6			R131	2C1
O	R121	2B2			SCB10	2F7			RPH1	2B0
E	B120	2F2			B040	2F5			BPH0	2F0
F	B110	2F2			B140	2F1			B150	2F1
G	SP6	3E7			B130	2G1			B050	2F5

CAPACITOR

	DESIG	CODE
	C1	600A,1
[4]	C2-C5	601A,5
[23]	C6-C28	KS-19774 L5,0.1

DIODE

DESIG	CODE
CR1	~~1N5225B~~ KS-21761 L1

RESISTOR

	DESIG	CODE
[4]	R1-R4	KS-20616 L1A,100
[4]	R5-R8	↓ ,511
[4]	R9-R12	,39
	R13	KS-20616 L1A,33

TRANSFORMER

	DESIG	CODE
[4]	T1-T4	2664G

CIRCUIT DESCRIPTION

THIS PACK CONTAINS A 21-BIT SHIFT REGISTER TO RECEIVE A SERIAL MESSAGE FROM THE 3ACC. BIPOLAR PULSES ARE RECEIVED FROM EITHER CC VIA THE A OR B INPUT PORTS. CHLS CONVERTS THE RECEIVED PULSES TO TTL LEVELS. THE CLOCKPULSE (RSHP1) RECOVERED FROM THE BITSTREAM IS NOMINALLY 75 NSEC WIDE. THE RECOVERED DATA (DTAIN1) IS HELD STABLE OVER THE TRAILING EDGE OF THE RSHP1 PULSE BY THE DTR F/F.

THE 21-BIT MESSAGE IS CHECKED FOR SINGLE ERRORS BY THE PARITY CHECK F/F (SPCHK). A STOP LATCH IS SET WHEN THE FIRST ONE BIT IS CLOCKED INTO THE IOBA F/F. THE SHIFT REGISTER CONTENTS ARE FROZEN BECAUSE THE REGISTER IS SET INTO THE PARALLEL LOAD MODE. 20-BITS OF THE REGISTER ARE AVAILABLE FOR DECODING PURPOSES. THE STATES OF THE 19 INPUT LEADS ARE LOADED INTO THE REGISTER AT THE TRAILING EDGE OF A PULSE ON LEAD PLIOBO TO SEND THE 21-BIT MESSAGE BACK TO THE CC THE ENR F/F IS RESET BY A HIGH INPUT ON LEAD STRTR1. THE ENR F/F ENABLES THE REPLY MESSAGE MODULATOR RMM AND PLACES THE REGISTER INTO THE SERIAL SHIFT MODE. THE DATA APPEARING AT THE OUTPUT OF IOBA (DTAOTO) MODULATES THE TWO CLOCKPULSES TO GENERATE BIPOLAR PULSES AT THE A OR B OUTPUT PORTS.

THE CIRCUIT IS INITIALIZED BY A HIGH INPUT ON LEAD RSETD1. R13 AND CR1 GENERATE THE 3-VOLT SUPPLY REQUIRED BY THE 175H LEVEL SHIFTERS CHLS.

ISSUE
2B1

JK6 CIRCUIT PACK
②

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CPS-JK6
SHEET 4

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